	U	P	1	2	3	4	5	Document ID	Issue Date	Inventor
1	☐	☐	☐	☐	☐	☐	☐	US 6278164 B1	20010821	Hieda, Katsuhiko et al.
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1. A ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions,

said first gate intermediate layer also extending in the direction of the line running between said source/drain regions,

said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode ~~connected~~ to said second gate electrode.

2. The ferroelectric transistor according to claim 1, wherein: said second gate intermediate layer includes two substructures configured mirror-symmetrically in relation to said first gate intermediate layer; said second gate electrode includes two substructures configured mirror-symmetrically in relation to said first gate intermediate layer; and said two substructures of said second gate electrode are electrically connected to each other.

3. The ferroelectric transistor according to claim 2, wherein said first gate intermediate layer includes a dielectric layer configured between said surface of said semiconductor substrate and said ferroelectric layer.

4. The ferroelectric transistor according to claim 1, wherein said first gate intermediate layer includes a dielectric layer configured between said surface of said semiconductor substrate and said ferroelectric layer.

5. The ferroelectric transistor according to claim 4, wherein said dielectric layer of said first gate intermediate layer and said dielectric layer of said second gate intermediate layer a re formed as a continuous dielectric layer.

6. The ferroelectric transistor according to claim 1, comprising a diode structure connecting said first gate electrode to said second gate electrode, said diode structure including an electrode selected from the group consisting of said first gate electrode and said second gate electrode.

7. The ferroelectric transistor according to claim 5, wherein; said first gate electrode includes polycrystalline silicon including doping of a first conductivity type; said second gate electrode includes polycrystalline silicon including doping of a second conductivity type that is opposite said first conductivity type; and said first gate electrode adjacent said second gate electrode.

8. The ferroelectric transistor according to claim 1, comprising an auxiliary layer disposed between said ferroelectric ~~layerand~~ **layer and** said first gate electrode.

9. The ferroelectric transistor according to claim 1, wherein: said first gate intermediate layer includes a material selected from the group consisting of CeO.sub.2, ZrO.sub.2, Y.sub.2O.sub.3, and SrTiO.sub.3; said second gate intermediate layer includes a material selected from the group consisting of SiO.sub.2, CeO.sub.2, ZrO.sub.2, and

SrTiO.sub.3; said ferroelectric layer includes a material selected from the group consisting of strontium-bismuth-tantalum, lead-zirconium-titanate, lithium-niobate and barium-strontium-titanate; and said semiconductor substrate includes monocrystalline silicon.

10. The ferroelectric transistor according to claim 1, wherein said first gate electrode and said second gate electrode form a diode structure.

11. A memory cell configuration including a plurality of memory cells, each one of said plurality of said memory cells including a ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions,

said first gate intermediate layer also extending in the direction of the line running between said source/drain regions,

said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode ~~connected~~ to said second gate electrode.

12. The memory cell configuration according to claim 11, comprising: a plurality of bit lines, a plurality of supply lines, and a plurality of word lines crossing said plurality of said supply lines and said plurality of said bit lines; each one of said plurality of said memory cells including a selection transistor connected between said second gate electrode of said ferroelectric transistor of the one of said plurality of said memory cells and one of said plurality of said supply lines, said selection transistor of each one of said memory cells including a control electrode connected to one of said plurality of said word lines; and said ferroelectric transistor of each one of said plurality of said memory cells connected between adjacent ones of said plurality of said bit lines.